IN THE CLAIMS:

Please amend claims 1, 3 and 7 as indicated in the complete claims listing provided below.

1. (currently amended) A method of clocking an IP core ~~during~~ and an emulated design, in conjunction with carrying out a debugging operation, comprising:

clocking a design mapped onto an emulator to test the design;

clocking the IP core with the same clock used for testing the design mapped onto the emulator; and

~~characterized by~~ upon a start of the debugging operation switching the clocking of the IP core from ~~a~~ the clock used for testing ~~a~~ the design mapped onto ~~an~~ the emulator to a second clock source comprising a clock oscillator or any free-running clock source, for carrying out the debugging operation.

2. (previously amended) The method of claim 1, wherein said switching is to said clock oscillator, which is provided on an IP-Xpress board.

3. (currently amended) The method of claim 1, wherein the clock used for testing the design is either:

a) a clock sourced from the design mapped into the emulator;

b) a clock sourced directly from ~~the emulators~~ a clock generator circuit of the emulator; or

c) a clock oscillator locally mounted on ~~the~~ an IP-Xpress daughter board, or any free running clock source.

4. (previously amended) The method of claim 1, comprising the step of monitoring signals specific to the IP core which indicate a breakpoint in order to detect the breakpoint.

5. (previously amended) The method of claim 4, wherein said switching is performed upon detecting that the breakpoint has been entered.

6. (previously amended) The method of claim 1, wherein the IP core is a microprocessor or a DSP.

7. (currently amended) A system for clocking an IP core ~~during~~ and an emulated design, in conjunction with carrying out a debugging operation, comprising:

a first clock for clocking a design mapped onto an emulator to test the design, and to concurrently clock the IP core;

switching means;

a second clock source comprising a clock oscillator or any free-running clock source; and

control means for sending a control signal to the switching means when ~~the~~ a debugging operation is started, ~~for switching~~ said control signal causing the switching means to switch clocking of said IP core from said first clock to said second clock source for carrying out the debugging operation~~to the clock oscillator or any free-running clock source~~.